ADS5120EVM

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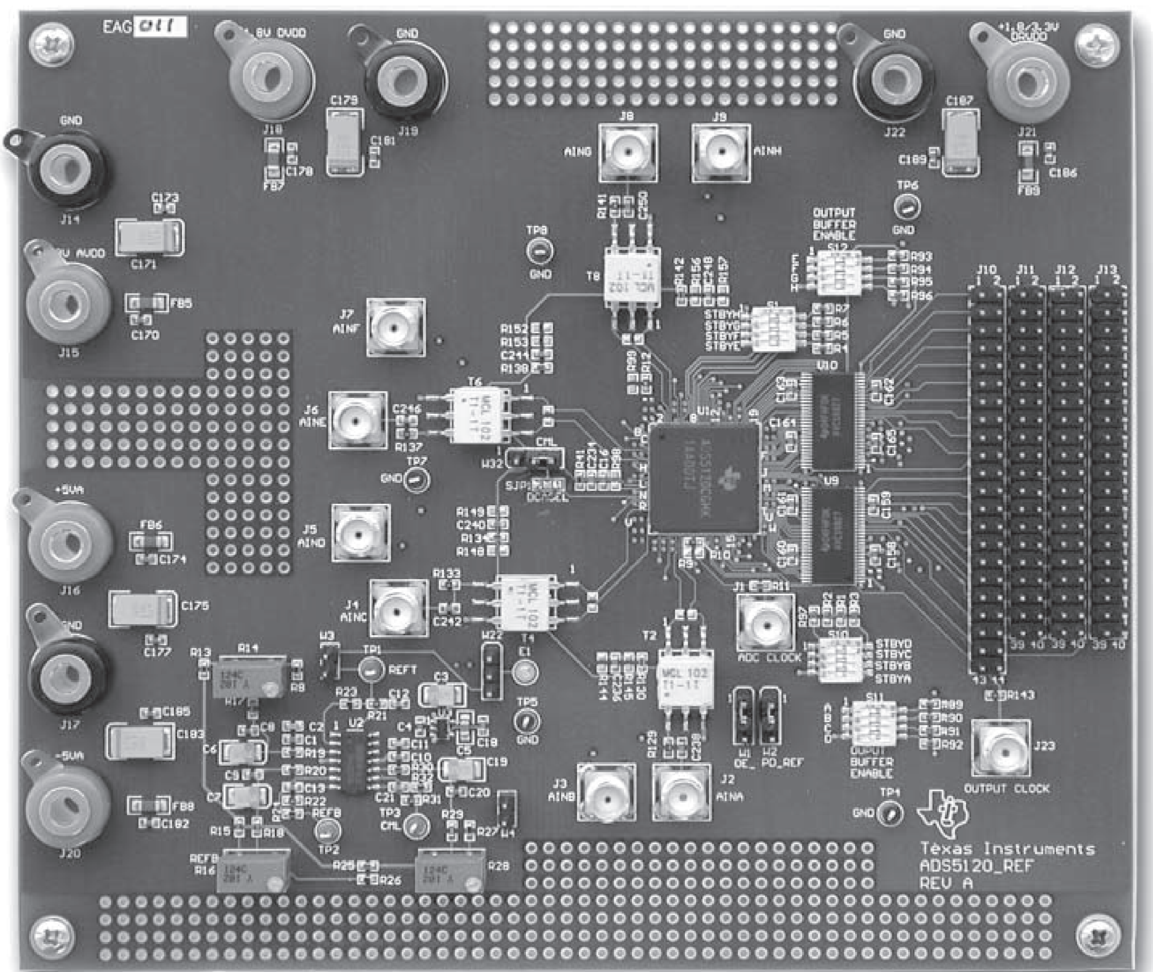

FEATURES

- FULLY POPULATED EVM
- PROVIDES FAST AND EASY PERFORMANCE TESTING FOR THE ADS5120
- DIFFERENTIAL TRANSFORMER-COUPLED INPUT CONFIGURATION FOR EACH CHANNEL
- EXTERNAL REFERENCE OPTION

DESCRIPTION

This user's guide describes the function and operation of the ADS5120 evaluation module. It is designed for ease of use when evaluating the high-speed Analog-to-Digital Converter (ADC) ADS5120. The ADS5120 is an 8-channel, simultaneous sampling 10-bit A/D converter sampling at up to 40MSPS. The evaluation module is completely assembled and provides a transformer-coupled input configuration for each of the channels. The ADS5120 operates on a 1.8V single supply. Optionally, the output logic buffers can be configured for 3.3V supply.

OVERVIEW

This preliminary User's Guide document gives a general overview of the ADS5120 evaluation module (EVM), and provides a general description of the features and functions to be considered while using this module.

The ADS5120EVM provides a platform for evaluating the ADS5120 ADC under various signal, reference, and supply conditions.

EVM BASIC FUNCTIONS

Analog inputs to the ADC are provided via eight SMA connectors (AINA…AINM). The single-ended inputs are transformer coupled and converted into differential signals at the inputs of the ADC.

The EVM provides a SMA connection for the ADC clock. A second SMA connector provides a clock to the output connector. This allows the user to provide the required setup and hold times of the output data with respect to the output clock. Refer to the Clock input section for proper configuration and operation.

Digital outputs from the EVM are via four connectors. The digital lines from the ADC are buffered before going to these connectors. More information on these connectors can be found in the ADC Outputs section.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the analog and digital supplies.

In addition to the internal reference provided by the ADS5120 device, options are provided on the EVM to allow adjustment of the ADC references via an onboard reference circuit. A precision-voltage reference source, a resistor network, and an op amp provide the ADS5120 device reference voltages, top reference (REFT) and bottom reference (REFB).

POWER REQUIREMENTS

The EVM can be powered directly with a single +1.8V supply if using internal reference source and +1.8V logic outputs. +3.3V is required for the DRV_{DD} power input to provide +3.3V logic outputs. ±5V is required if using the onboard external reference circuit. Provision has also been made to allow the EVM to be powered with independent +1.8V analog and digital supplies to provide higher performance.

Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Under-voltage may cause improper operation of some or all of the EVM components.

ADS5120EVM OPERATIONAL PROCEDURE

A basic setup procedure that can be used as a board confidence check is as follows:

1) Verify all jumper settings against the schematic jumper list in Tables I and II:

JUMPER	FUNCTION	INSTALLED	REMOVED	DEFAULT
W3	REFT Feed	External	Internal	Removed
W4	REFB Feed	External	Internal	Removed
R9	ADC Clock Termination Option	Provide Pull-Up Termination	No Pull-Up Termination	Removed

TABLE I. 2-Pin Jumper List.

2) Connect supplies to the EVM as follows: +1.8V analog supply to J15 and return to J14. +1.8V digital supply to J18 and return to J19. +1.8V driver supply to J21 and return to J22.
3) Switch power supplies ON.
4) Use a function generator with 50Ω output impedance to input a 40MHz, 1.5V offset, 3Vp-p amplitude square wave signal into J1 to be used as the ADC clock. The frequency of the clock must be within the specification for the device speed grade.
5) Use a function generator with 50Ω output impedance to input a 40MHz, 1.5V offset, 3Vp-p amplitude square wave signal into J23 to be used as the buffered output clock. This signal must be the same frequency and synchronized with the ADC clock.
6) Use a frequency generator with 50Ω output impedance to input a 1.5MHz, 0V offset, 0.4Vp-p amplitude sine wave signal into analog input SMA J2. This will provide a transformer-coupled differential signal to channel A of the ADC.
7) The digital pattern on the output connector J11 should now represent a sine wave and can be monitored using a logic analyzer.

JUMPER	FUNCTION	LOCATION: PINS 1-2	LOCATION: PINS 3-4	DEFAULT
W32	Transformer Common-Mode Select	External Common-Mode Voltage	ADC Common-Mode Voltage	2-3
W2	Power-Down Internal Reference	Internal Reference Operational	Internal Reference Powered Down	1-2
W1	Output Data Enable	ADC Outputs Enabled	ADC Outputs Tri-Stated	1-2
W22	Bandgap Input Voltage (power-down reference mode)	1.3V	REFT Voltage	Removed
SJP1	ADC Duty-Cycle Adjust Enable	Enabled	Disabled	2-3

TABLE II. 3-Pin Jumper List.

CIRCUIT DESCRIPTION

ANALOG INPUTS

The ADC receives differential inputs from eight transformers. The eight single-ended inputs are provided via SMA connectors J2, J3, J4, J5, J6, J7, J8, and J9. The inputs are AC-coupled and have 50Ω termination resistors.

External Reference Inputs

In addition to being able to use the internal reference of the ADC, a reference circuit has been included on the EVM. Using a precision +2.5V low-noise linear regulator as the primary source, this circuit allows adjustment of the REFT and REFB signals to the ADC using potentiometers R14 and R16, respectively. A third source, CML, is also generated to provide an adjustable common-mode voltage to be used by the transformers during external reference operation. CML is adjusted by potentiometer R28. In order to use the ADC with external references, install jumpers W3 and W4, install jumper W32 between pins 1 and 2 and jumper W22 between pins 2 and 3. If REFT is set to any voltage other than 1.32V, jumper W22 should be installed between pins 1 and 2 for optimal ADC performance. The ranges of the external reference signals are shown in Table III.

SIGNAL	MINIMUM VOLTAGE	TYPICAL VOLTAGE	MAXIMUM VOLTAGE
REFT	0.9	1.32	1.6
REFB	0.3	0.781	0.9
CML	0.5	1.05	1.25

TABLE III. Reference Voltage Adjustment Ranges.

Clock Inputs

The EVM provides separate clock inputs for the ADC (“ADC Clock”) and the output buffer (“Output Clock”). This allows the user to send a modified version of the ADC clock (inverted, delayed, ect.) with the output data to generate the required setup and hold times for the user’s interface.

An adjustment in the placement of the output clock that captures the data relative to the ADC clock may be neccessary depending on the specific timing requirements of the logic analyzer used. If poor performance is observed, verify the correct timing.

The ADC clock input is SMA connector J1 and has provisions for serial and/or parallel termination. The buffered output clock input is SMA connector J23. The clock inputs should be 50Ω square wave signals, +1.8V or +3.3V referenced to ground (based on DRV_{DD} voltage).

Control Inputs

The ADC has three discrete inputs to control the operation of the device:

Standby

The ADC has individual standby control inputs for each of the eight output data buses. These are controlled by the two dip switches, S1 and S10. Table IV shows switch operation.

SWITCH	CHANNEL	SWITCH OPEN	SWITCH CLOSED
S1-1	H	Operate	Standby
S1-2	G	Operate	Standby
S1-3	F	Operate	Standby
S1-4	E	Operate	Standby
S10-1	D	Operate	Standby
S10-2	C	Operate	Standby
S10-3	B	Operate	Standby
S10-4	A	Operate	Standby

TABLE IV. Standby Switch Operation.

Duty-Cycle Adjust

With jumper SJP1 installed between pins 2 and 3, the internal duty cycle adjust circuit is disabled. Installing SJP1 between 1 and 2 enables the internal duty cycle adjust circuit. See device data sheet for details.

Output Enable

With jumper W1 installed between pins 1 and 2, the ADC data outputs are enabled. The outputs are tri-stated with W1 between pins 2 and 3.

Output Buffer Enables

DIP switch S11 controls the ‘Enable’ function of the SN74AVC16827 buffers for channels A, B, C, and D. DIP switch S12 controls the ‘Enable’ function of the SN74AVC16827 buffers for channels E, F, G, and H. With the DIP switch set to the open position, the buffer outputs are enabled. With the switches set to the closed position, the outputs are tri-stated. Table V shows individual switch operation.

SWITCH	CHANNEL	SWITCH CLOSED	SWITCH OPEN
S11-1	A	Tri-State	Operate
S11-2	B	Tri-State	Operate
S11-3	C	Tri-State	Operate
S11-4	D	Tri-State	Operate
S12-1	E	Tri-State	Operate
S12-2	F	Tri-State	Operate
S12-3	G	Tri-State	Operate
S12-4	H	Tri-State	Operate

TABLE V. Output Buffer Switch Operation.

Power-Down Reference

With jumper W2 installed between pins 2 and 3, the ADC internal reference is disabled and the device is in external reference mode. The ADC is in internal reference mode with jumper W2 installed between pins 1 and 2.

Power

Power is supplied to the EVM via banana jack sockets. A separate connection is provided for a +1.8V analog supply (J15 and J14), +1.8V digital supply (J18 and J19), +1.8/3.3V digital driver supply (J21 and J22), and ±5V analog supply (J16, J17, and J20).

ADC Outputs

The data outputs from the ADC are buffered using four SN74AVC16827 buffers before going to headers J10, J11, J12, and J13. The ADC and output buffer can provide +1.8V or +3.3V output levels. This is selected by the voltage placed at the ADC driver supply (banana jacks J21 and J22). The standard headers are on a 100-mil grid, which allows for easy connection to a logic analyzer.

PHYSICAL DESCRIPTION

This section describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

PCB LAYOUT

The EVM is constructed on a 8-layer, 5.45" x 6.30", 0.062-inch thick PCB using FR-4 material. A brief description of the individual layers is shown below. The layer drawings are attached to the end of this document (Figures 6 - 13).

PARTS LIST

Table VI lists the parts used in constructing the EVM.

Value	Footprint	Qty	Part Number	Vendor	Digi-Key Number	REF DES	Not Installed
47µF, Tantalum, 10%, 10V	7343	5	10TPA47M	SANYO	PCS2476CT-ND	C171 C175 C179 C183 C187	
10µF, 10V, 10% Capacitor	3528	9	GRM42X5R106K10	Murata	PCS2106CT-ND	C3 C6 C7 C19 C172 C176 C180 C184 C188	
0.1µF, 10V, 10% Capacitor	402	47		Panasonic		C103-C106 C117 C118 C120 C137 C150-C153 C190-C192 C194 C195 C197-C215 C217 C219-C224 C226 C228 C230 C231	
0.1µF, 16V, 10% Capacitor	603	48	ECJ-1VB1C104K	Panasonic	PCC1762CT-ND	C1 C8-C10 C20 C154-C170 C173 C174 C177 C178 C181 C182 C185 C186 C189 C234-C250	
0.01µF, 50V, 10% Capacitor	603	3		AVX	PCC1750CT-ND	C14 C15 C18	
1.0µF, 10V, 10% Capacitor	603	4		AVX	PCC1787CT-ND	C4 C16 C17 C233	
15pF, 16V, 10% Capacitor	603	0					C22-C29
470pF, 16V, 10% Capacitor	603	2			PCC1955CT-ND	C2 C11	
2.2µF, 16V, 10% Capacitor	805	1			PCC1923CT-ND	C5	
0.047µF, 16V, 10%	603	3				C12 C13 C21	
Ferrite Bead	1206	5			P10437CT-ND	FB5-FB9	
0Ω Resistor	603	9				R11 R128 R130 R132 R134 R136 R138 R140 R142	R9 R98 R99
10kΩ Resistor, 1/16W, 1%	603	3			P10.0KHCT-ND	R17 R18 R29	
100Ω Resistor, 1/16W, 1%	603	3			P100YCT-ND	R19 R20 R30	
100kΩ Resistor, 1/16W, 1%	603	9				R33-R41	
1kΩ Resistor, 1/16W, 1%	603	3			P1.00KHCT-ND	R8 R13 R101	R145 R147 R149 R151 R153 R155 R157 R159
2.0kΩ Resistor, 1/16W, 1%	603	3				R23 R24 R32	
49.9Ω Resistor, 1/16W, 1%	603	13	ERJ-3EKF499R0V	Panasonic	P499HCT-ND	R10 R21 R22 R31 R127 R129 R131 R133 R135 R137 R139 R141 R143	
2.49kΩ Resistor, 1/16W, 1%	603	1	ERJ-3EKF249R0V	Panasonic	P2.49KHCT-ND	R15	
3.01kΩ Resistor, 1/16W, 1%	603	1	ERJ-3EKF301R0V	Panasonic	P3.01KHCT-ND	R102	
4.02kΩ Resistor, 1/16W, 1%	603	0	ERJ-3EKF402R0V	Panasonic	P4.02KHCT-ND		R144 R146 R148 R150 R152 R154 R156 R158
4.7kΩ Resistor, 1/16W, 1%	603	16	ERJ-3EKF4.7KR0V	Panasonic	P4.7KHCT-ND	R1-R7 R89-R97	
475Ω Resistor, 1/16W, 1%	603	2	ERJ-3EKF475R0V	Panasonic	P475HCT-ND	R26 R27	
6.04kΩ Resistor, 1/16W, 1%	603	1	ERJ-3EKF604KR0V	Panasonic	P6.04KHCT-ND	R12	
953Ω Resistor, 1/16W, 1%	603	1			P953GCT-ND	R25	
1k Pot	BOURNS_3296Y	3	3296Y-102	Bourns	3296Y-102-ND	R14 R16 R28	
Transformer	MC_KK81	8	T1-1T-KK81	Mini-Circuits		T1-T8	
SMA Connectors	SMA_Jack	10	713-4339	ALLIED		J1-J9 J23	J3
Black Test Point	Test_point	5	5011K	Keystone		TP4-TP8	
Red Test Point	Test_point	3	5000K	Keystone		TP1-TP3	
2POS_header	2pos_jumper	2	TSW-150-07-L-S	Samtec		W3 W4	
3POS_header	3pos_jumper	4	TSW-150-07-L-S	Samtec		W1 W2 W22 W32	
3POS_JUMPER SMT	SJP3	1				SJP1	
40-Pin Header	20X2X.1	3	TSW-120-07-L-D	Samtec		J11-J13	
44-Pin Header	22X2X.1	1				J10	
Red Banana Jacks	BANANA_JACK	5	ST-351A	ALLIED		J15 J16 J18 J20 J21	
Black Banana Jacks	BANANA_JACK	4	ST351B	ALLIED		J14 J17 J19 J22	
ADS5120	257_S-PBGA(GHK)	1	ADS5120	TI		U1	
OPA4227UA	14-SOP(D)	1	OPA4227UA	TI		U2	
TPS79225	5 SOT-23(DBV)	1	TPS79225DBVT	TI		U3	
SN74AVC16827(DGG)	56-TSSOP(DGG)	4	SN74AVC16827(DGG)	TI		U8-U11	
SWITCH 4POS_SMT	SWITCH_4POS_SMT	4				S1 S10 S11 S12	
Stand Off Hex (1/4 x 0.5")	4-40 screw	4	1902CK-ND	ALLIED			

TABLE VI. Parts List.

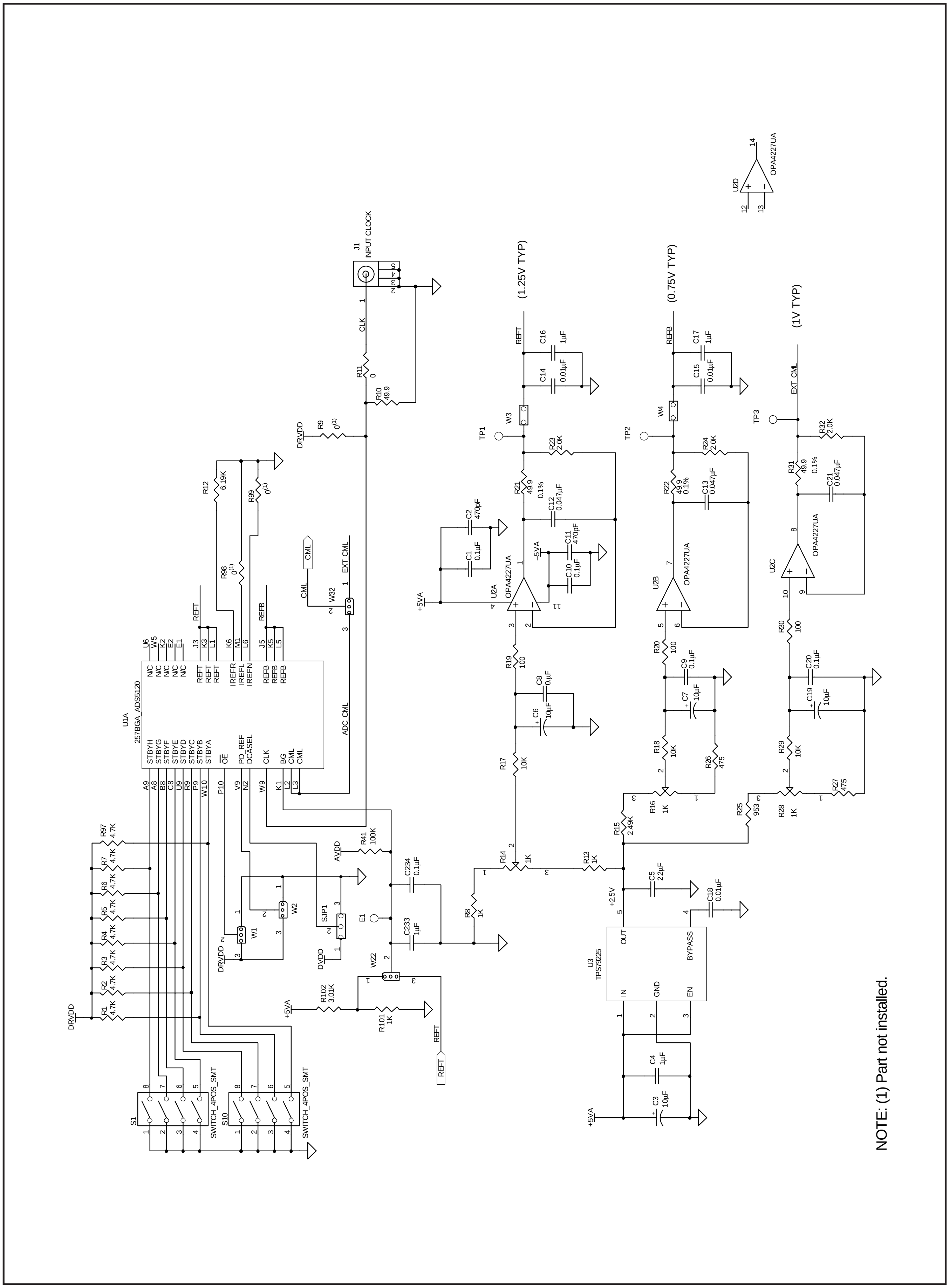

FIGURE 1. EVM Schematic Diagram (1 of 5).

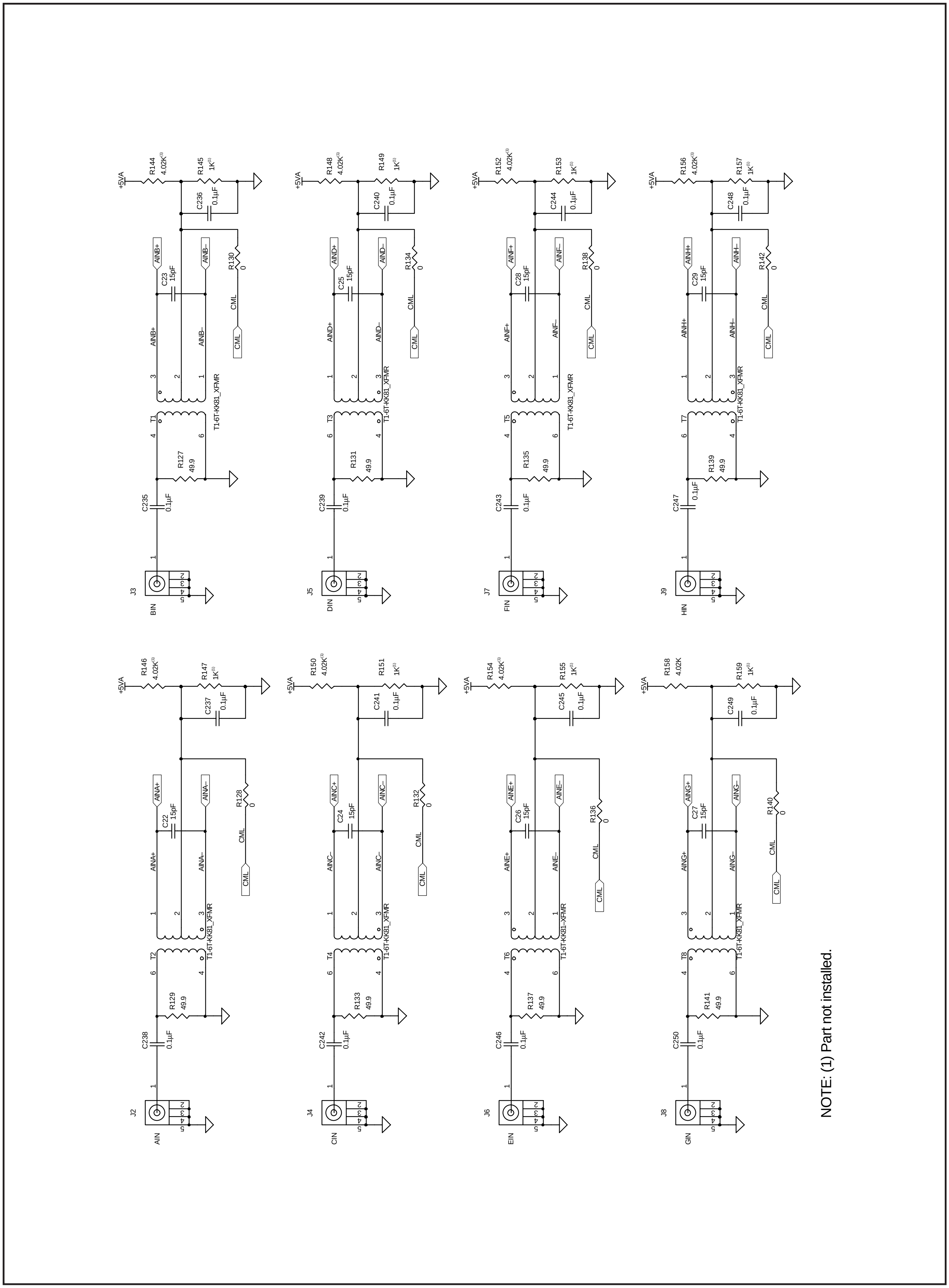

FIGURE 2. EVM Schematic Diagram (2 of 5).

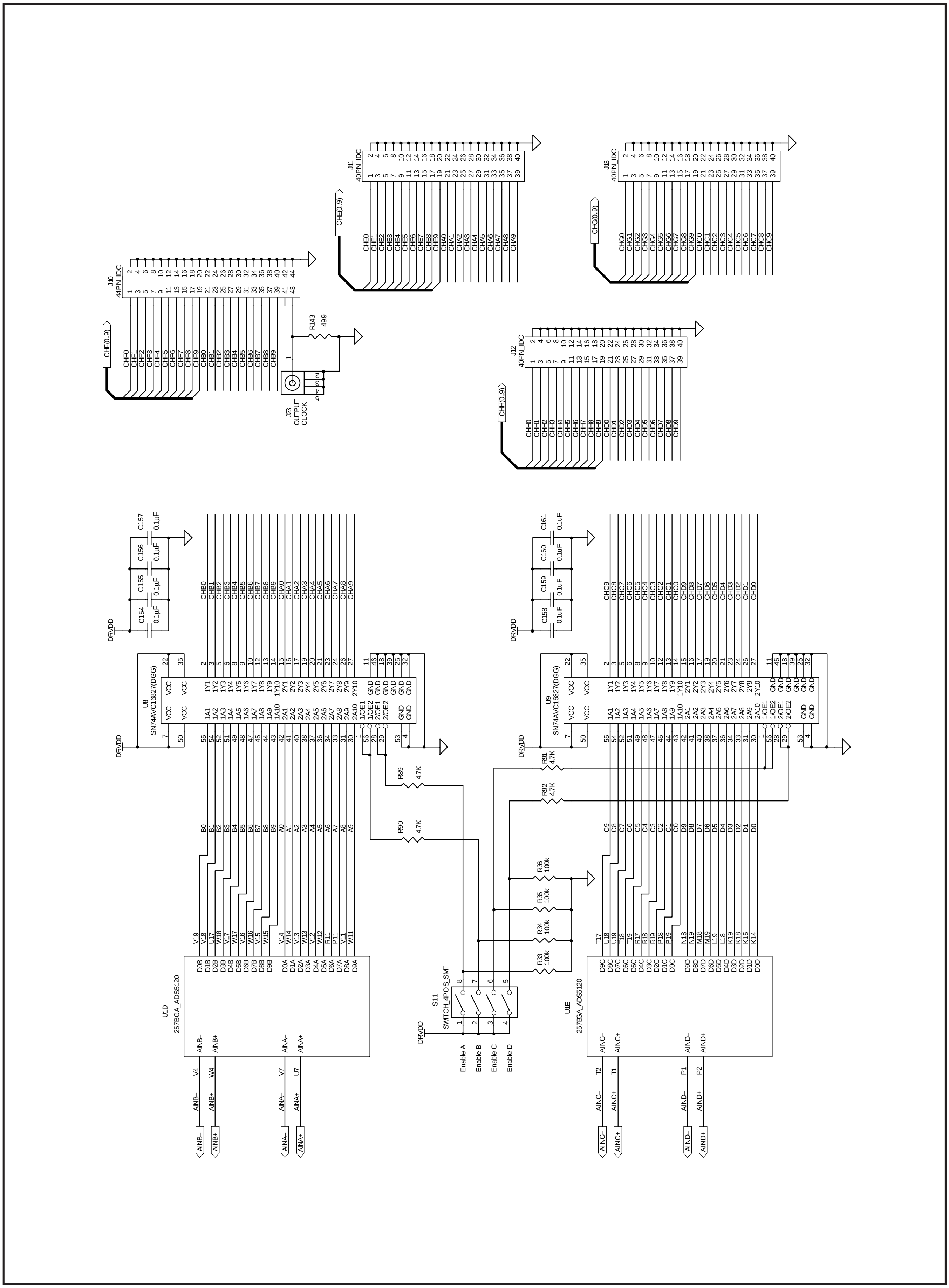

FIGURE 3. EVM Schematic Diagram (3 of 5).

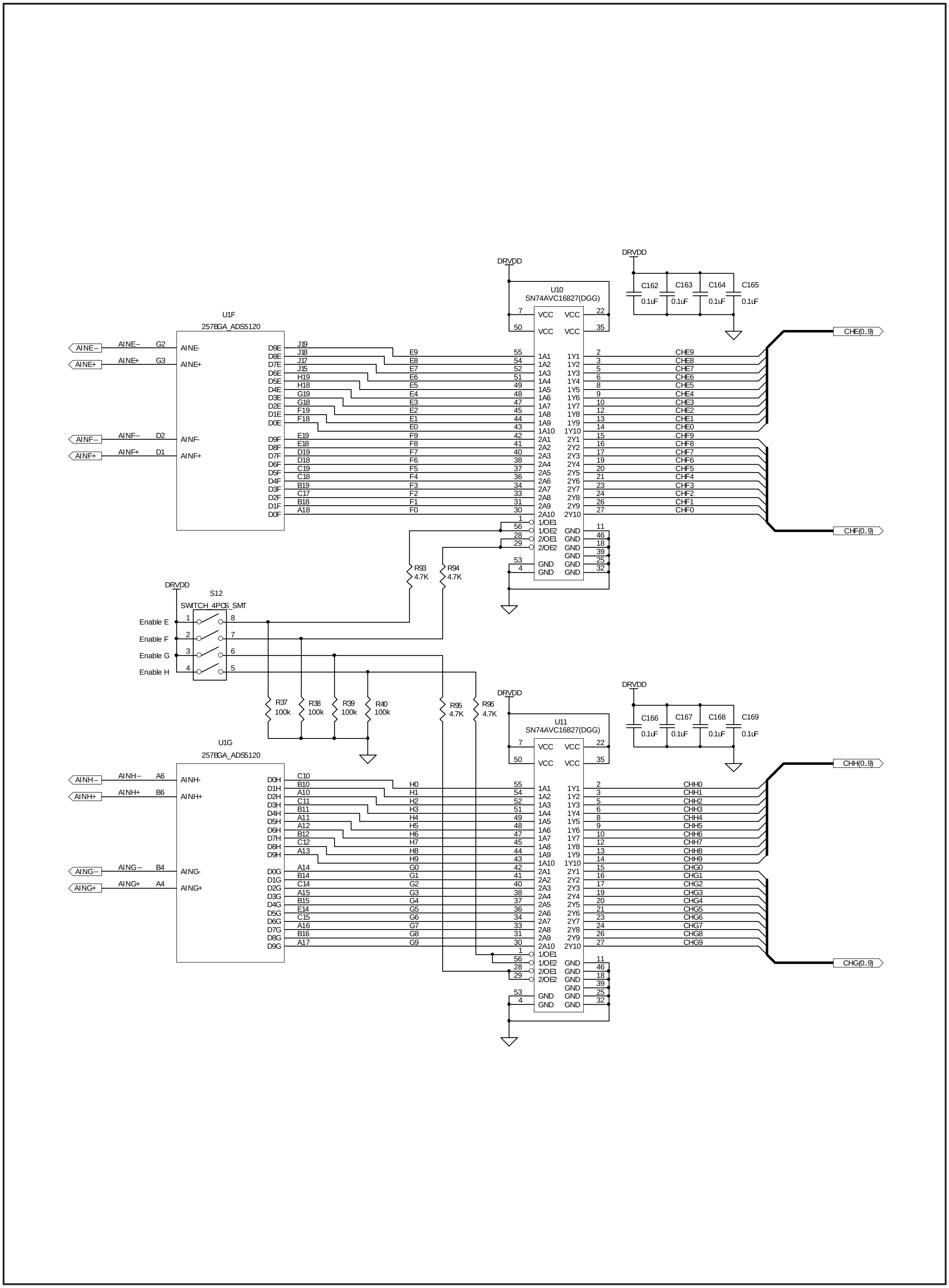

FIGURE 4. EVM Schematic Diagram (4 of 5).

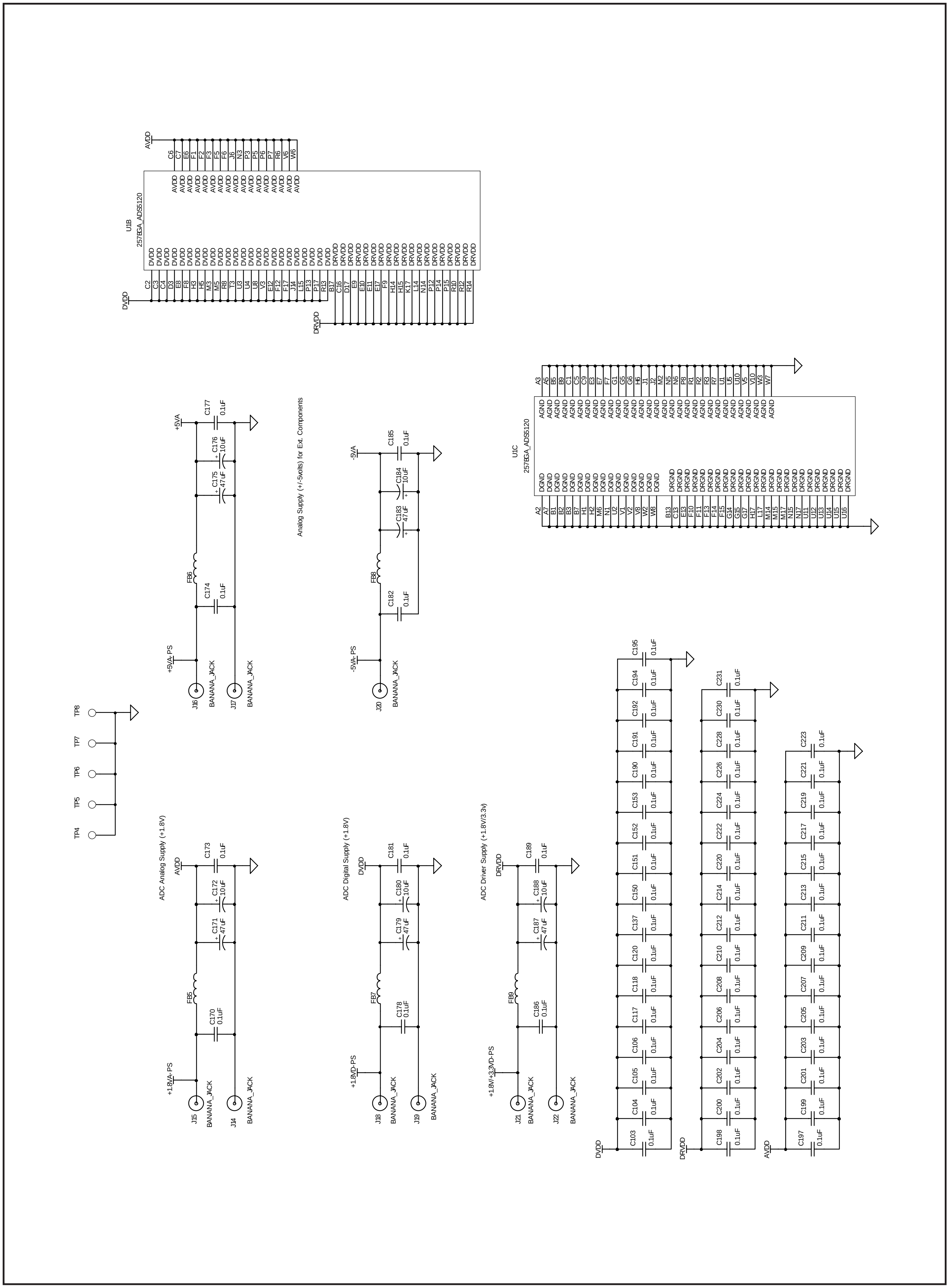

FIGURE 5. EVM Schematic Diagram (5 of 5).

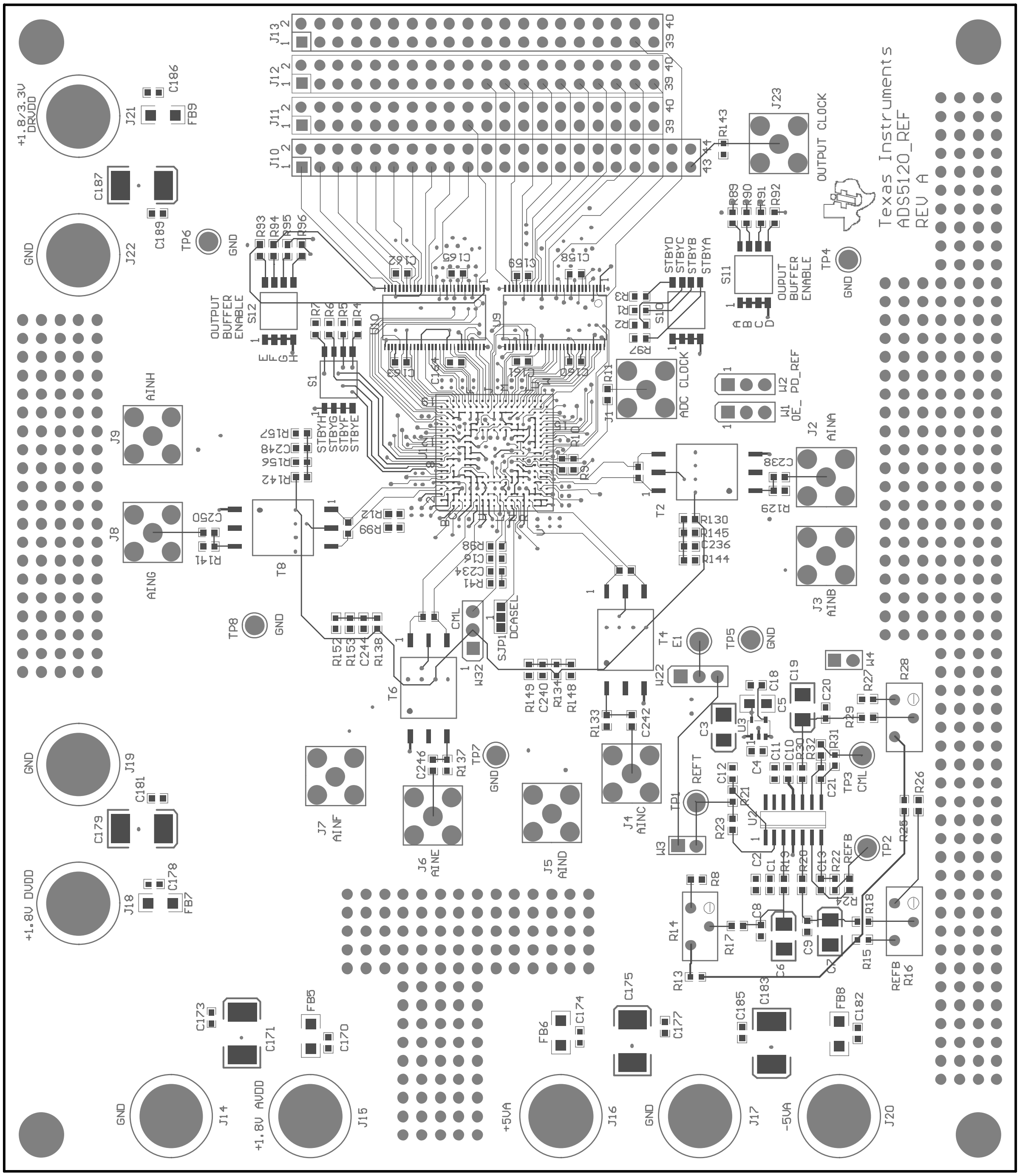

FIGURE 6. EVM Layer 1: Top Layer with Silk-Screen.

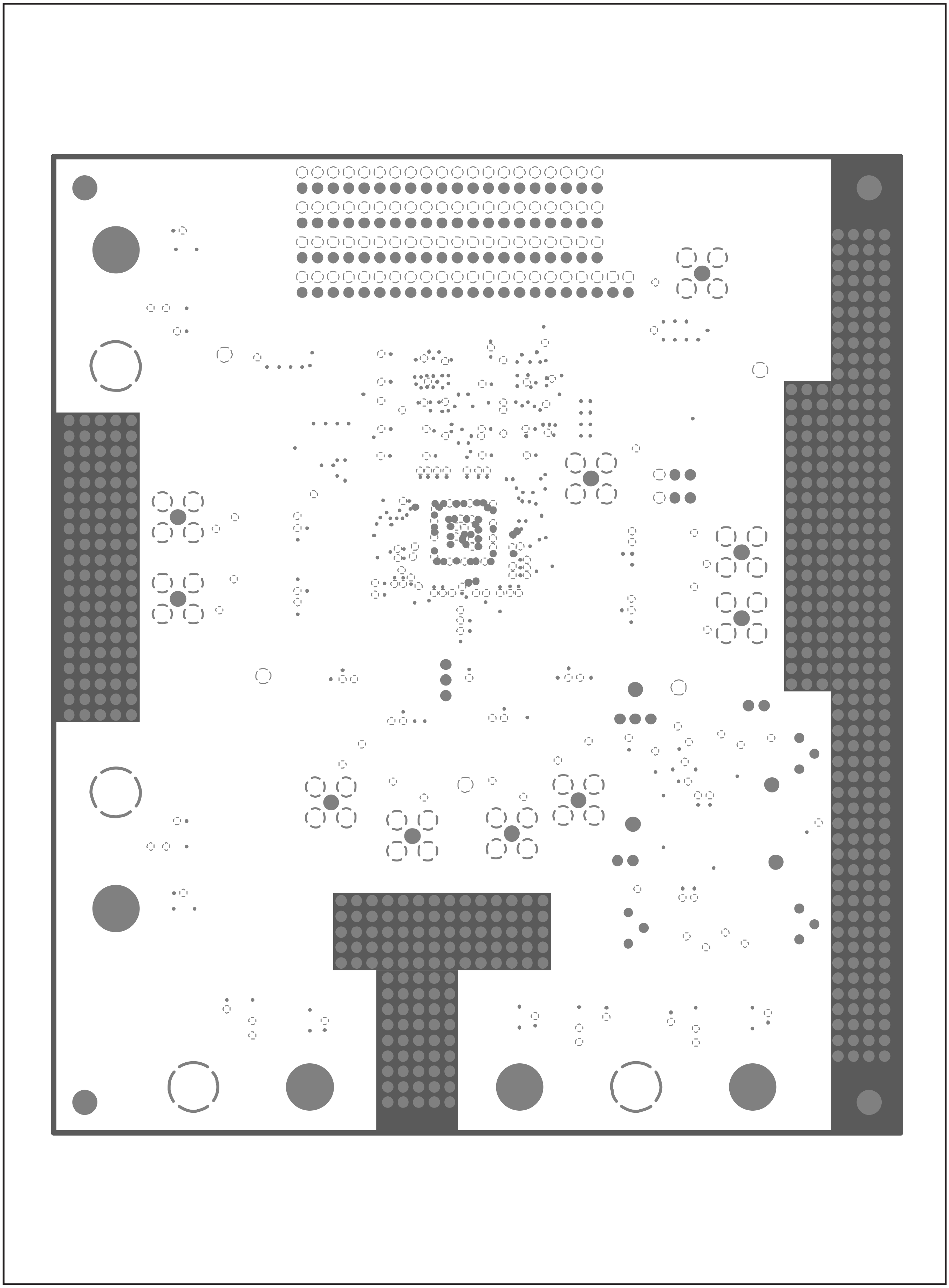

FIGURE 7. EVM Layer 2: Ground Plane I.

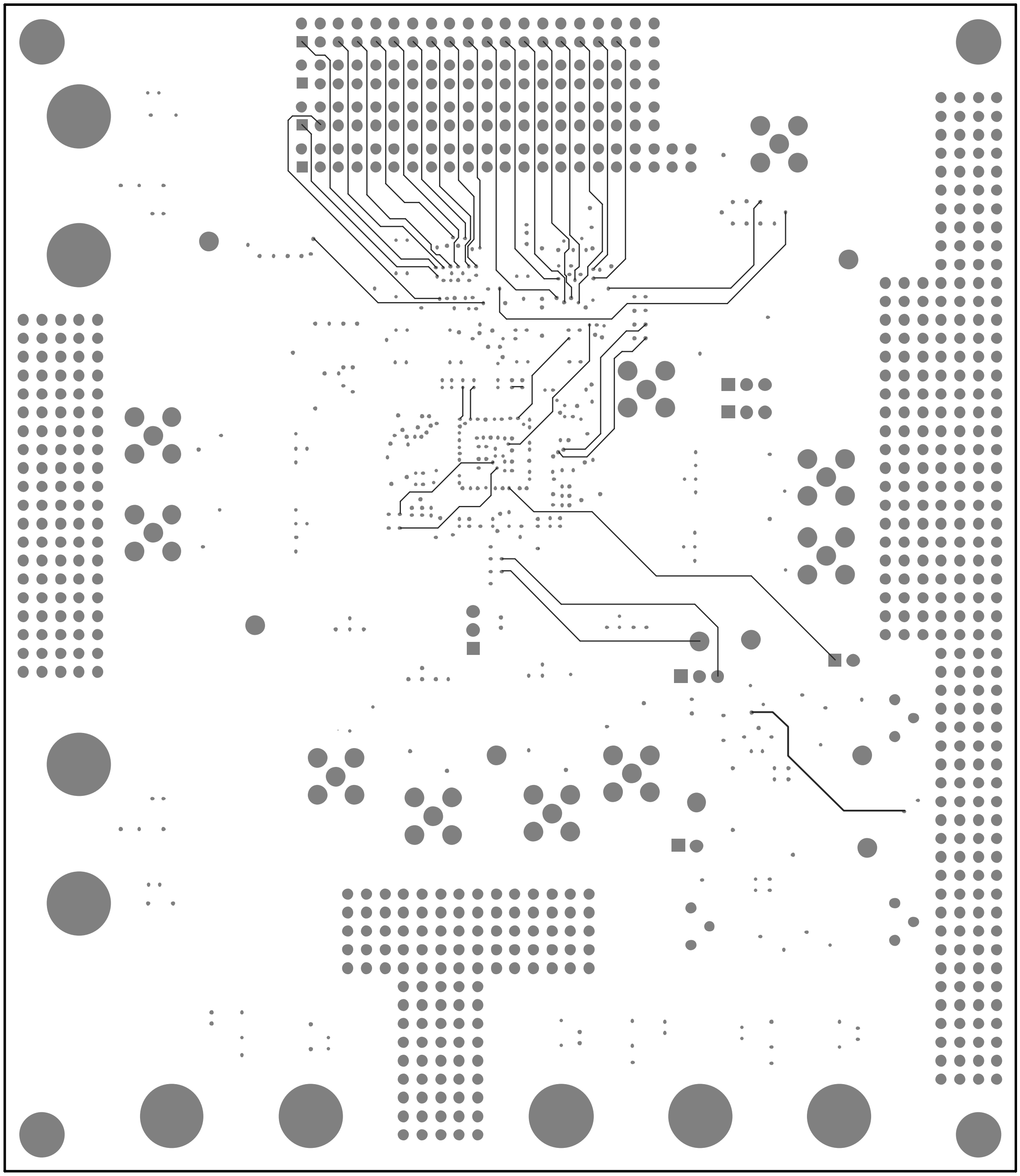

FIGURE 8. EVM Layer 3: Inner Layer I.

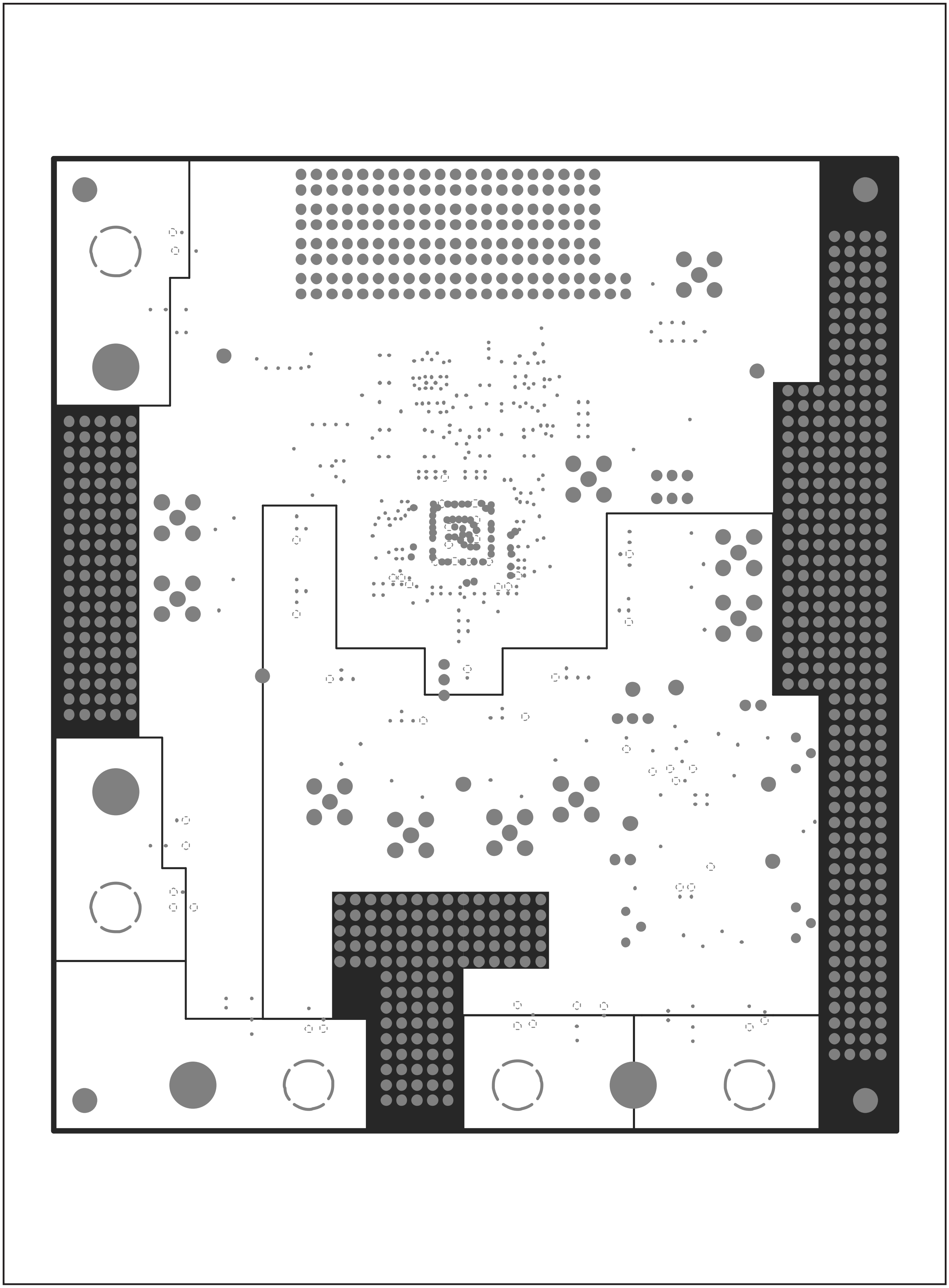

FIGURE 9. EVM Layer 4: Split Power Plane I.

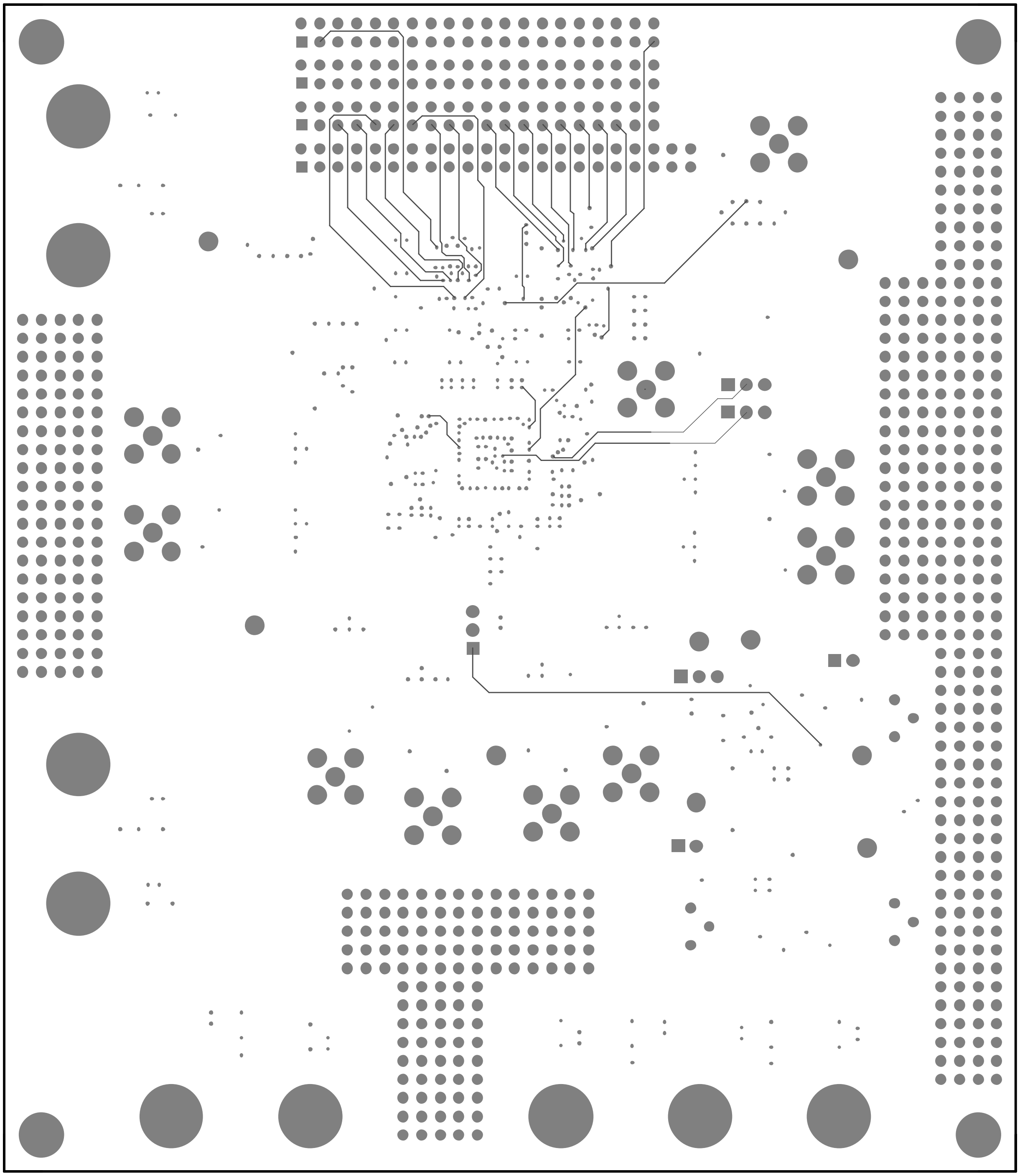

FIGURE 10. EVM Layer 5: Inner Layer II.

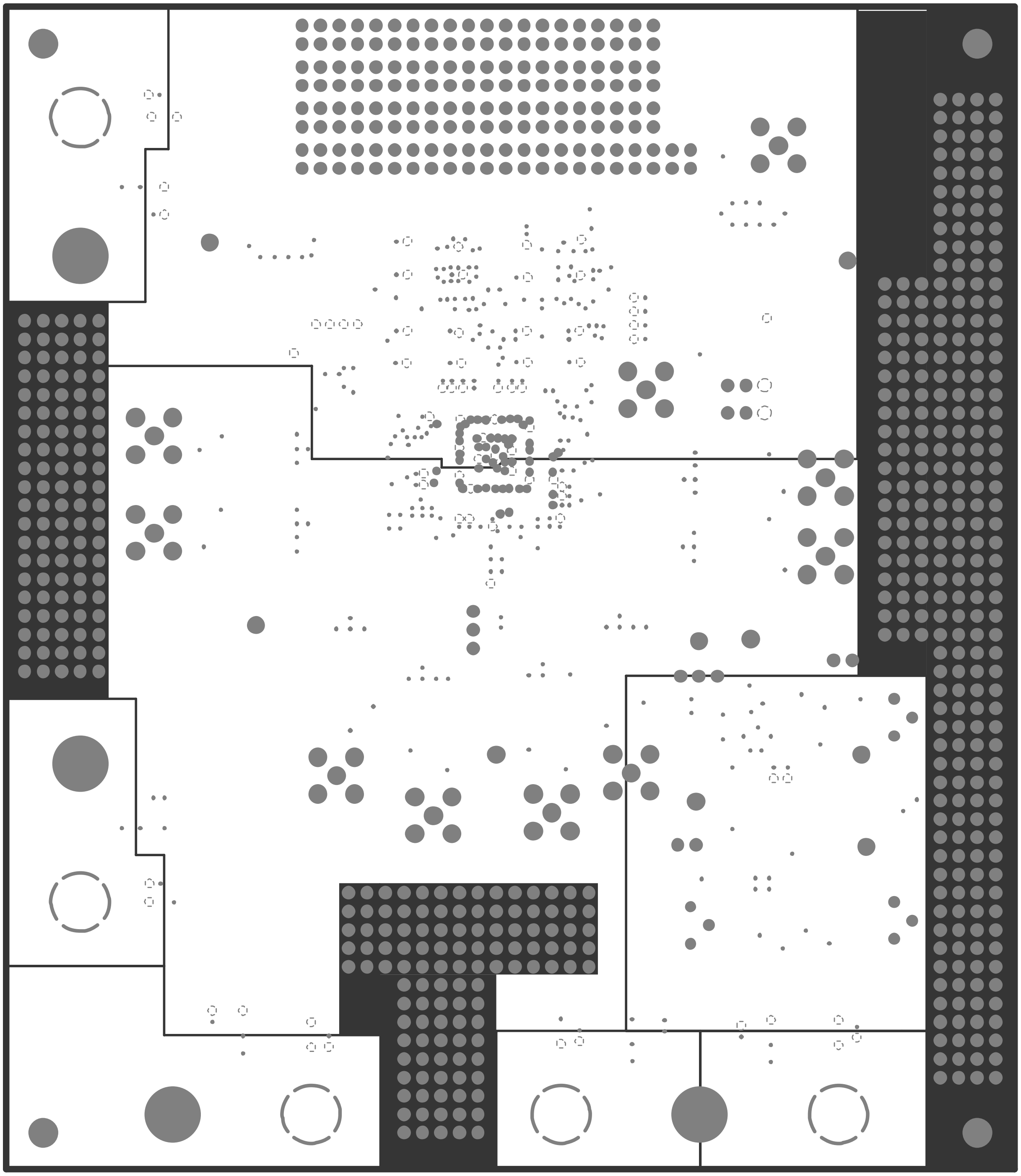

FIGURE 11. EVM Layer 6: Split Power Plane II.

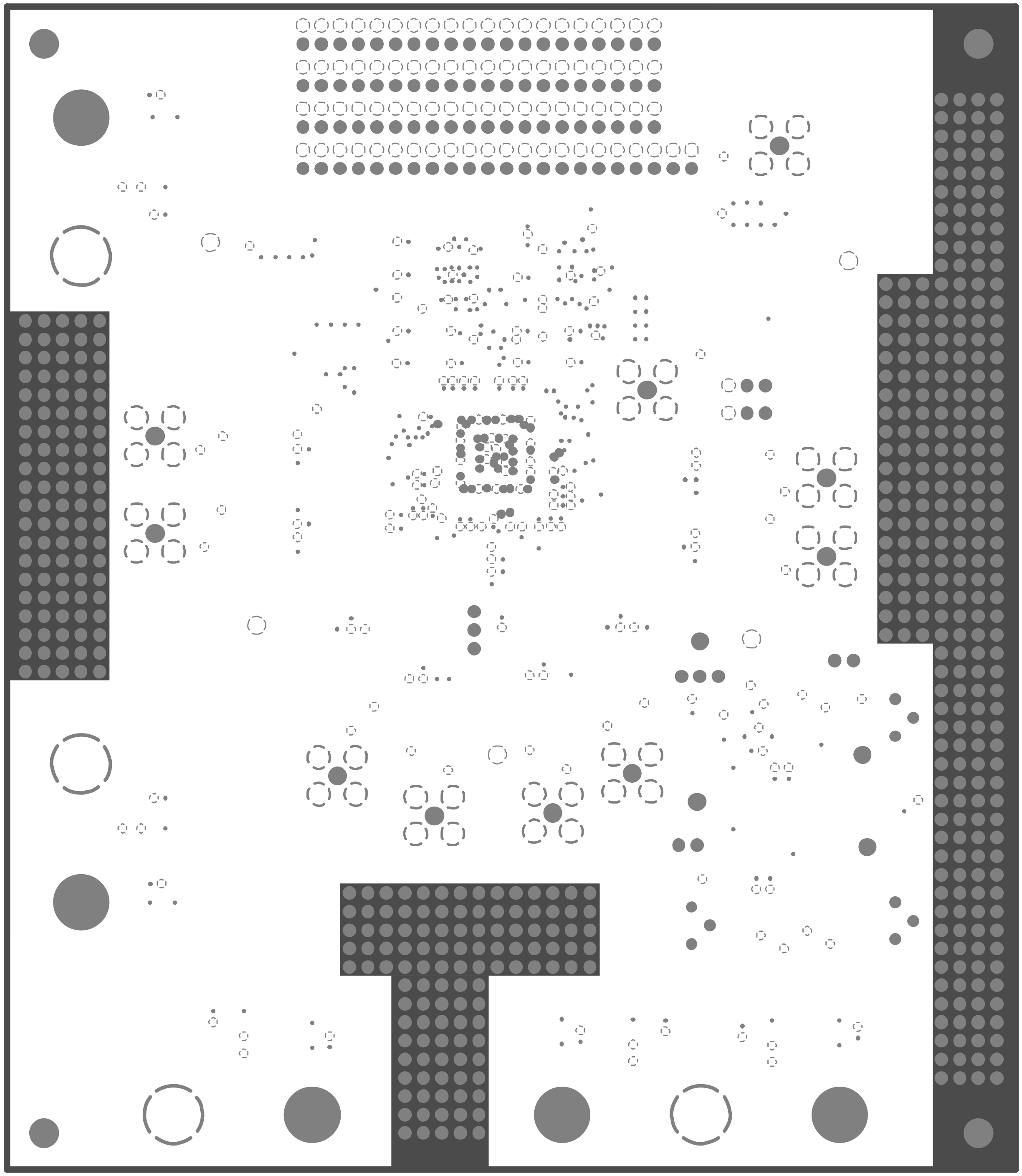

FIGURE 12. EVM Layer 7: Ground Plane II.

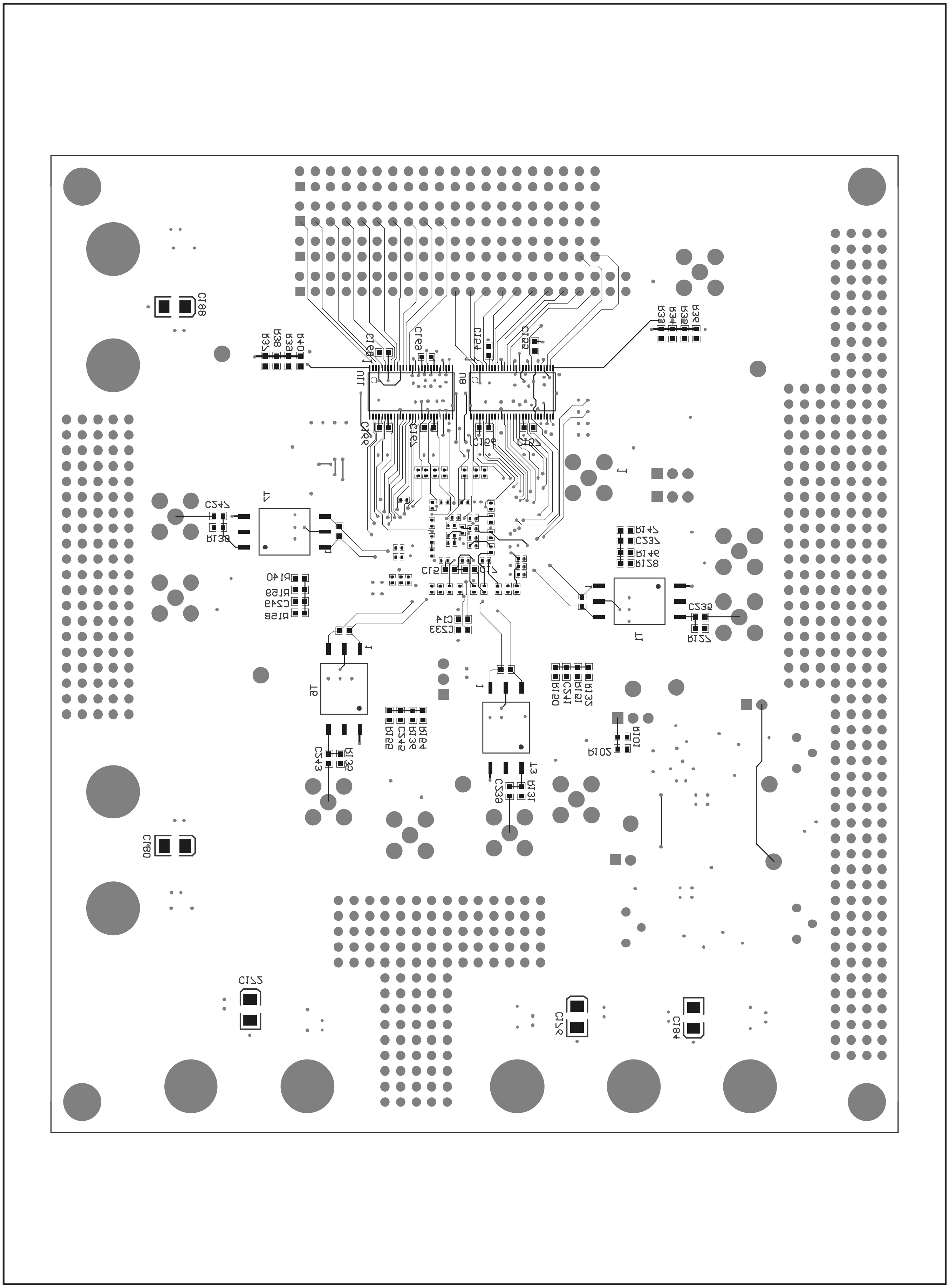

FIGURE 13. EVM Layer 8: Bottom Layer with Silk Screen.

EVM IMPORTANT NOTICE

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Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

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Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ≤ 3.3V and the output voltage range of ≤ 3.3V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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